OMNIRAM INTRODUCTION:

The Fulcrum Computer Products OMNIRAM for the IEEE 696/S-100 bus provides 64 kilobytes of fast static random access memory. Provision is made for 8 or 16-bit transfers, extended 24-bit addressing, and for control via the bus phantom line. In addition, a number of features are included to make the OMNIRAM compatible with systems designed before the IEEE-696 standard was developed. These include bank selection and provision for operation with IMSAI-type front panels. When the bank select option is activated, the board is divided into two parts which can reside in separate banks. The division of the board may be into two 32K sections or into one 16K section and one 48K section. Provision is made for DMA overide of bank select if needed. The board is also compatible with IMSAI-type extended addressing.

In the option selection sections which follow, the board is viewed from the component side. The edge opposite to the 100 pin S-100 bus connector is called the top and is so illustrated in all figures. All of the 8 sections of the dip switches are numbered from the top down, i.e. S1-1 is the section of S1 closest to the top of the card. Shorting of pin jumpers is accomplished with the shorting plugs supplied with the OMNIRAM. The symbol which appears in the following sections indicates that the two pins are shorted by one of the plugs.

EXTENDED ADDRESSING OPTION:

To enable 24-bit extended addressing short the two upper pins in jumper area G. To disable extended addressing short the lower top pins in jumper area G. One or the other of these two options MUST be selected. If extended addressing is selected, the 8 section dip switch S5 is used to select the extended address of the OMNIRAM. A16 is selected by section S5-1 while A23 is selected by section S5-8. If a switch section is ON (closed) logical address 0 has been selected for that address line. For example, to set the address of the OMNIRAM to 010000H, all of the sections of S5 should be in the ON position except for S5-1 which should be OFF.

G

enabled

G
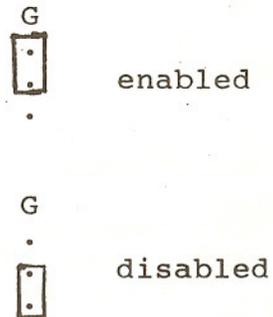
PHANTOM-IMSAI A16 OPTION:

To make the OMNIRAM respond to the phantom line, short the lower-right two pins in jumper area C (between U12 and U13). If this option is selected, pulling the phantom line low will disable the OMNIRAM. To enable IMSAI-type extended address line A16 short the two middle pins in jumper area C. To disable control by the phantom or IMSAI-type extended addressing short the upper-right two pins in jumper area C. One of these three options MUST be selected for the OMNIRAM to function correctly.

C phantom enabled

C IMSAI-A16 enabled

C option diabled
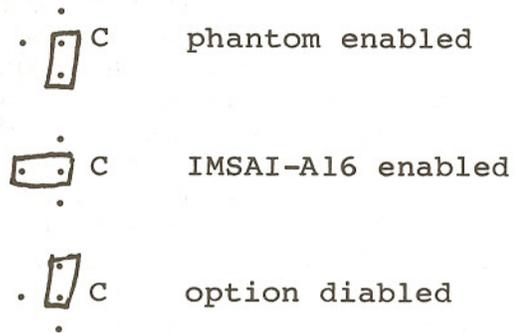
8/16 BIT TRANSFERS:

If this option is selected the OMNIRAM will respond to a sixteen bit transfer request on S-100 bus line 58 by pulling S-100 bus line 60 low and by reading or writing a sixteen bit word via the data bus lines. The pins in jumper area D and E are used to select this option. To select 16-bit transfers short the two pins in jumper area D and short the right two pins in jumper area E. 8-bit transfers in 16-bit systems may be forced by setting the jumpers as required for 8-bit systems. This option may be used to test by timing programs that 16-bit transfers are taking place.

D E 8-bit transfers
8-bit systems

D E 16-bit transfers
16-bit syste

D E 8-bit transfers
16-bit systems
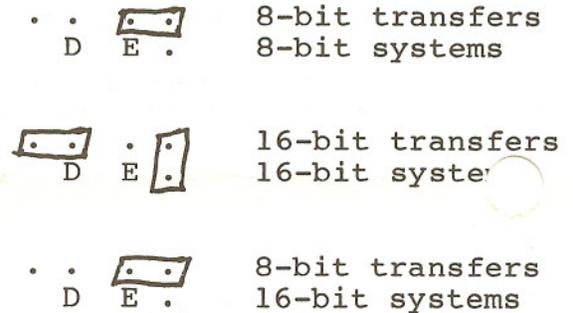
pDBIN/sMEMR OPTIONS:

This option is selected in jumper area F. The sMEMR option should be chosen. This is accomplished by shorting the upper two pins in the jumper area.

F normal position
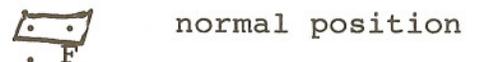
32K/64K BOARD OPTION:

Although the OMNIRAM is normally supplied as a 64K board, it may be desirable under certain circumstances to use only 32K of the board. The normal 64K configuration is activated by shorting the outer-most pairs of pins in jumper area H. If the 32K option is selected short the second and third pins from the top in area H. The address of the board will be determined by shorting or not shorting the lower two pins in that area. If these pins are shorted the lowest address of the OMNIRAM will be 0000H. If they are open, the lowest address will be 8000H. One of these options MUST be selected for the OMNIRAM to function correctly.

H

64K Option (normal)

H

32K Option (0000H)

H

32K Option (8000H)
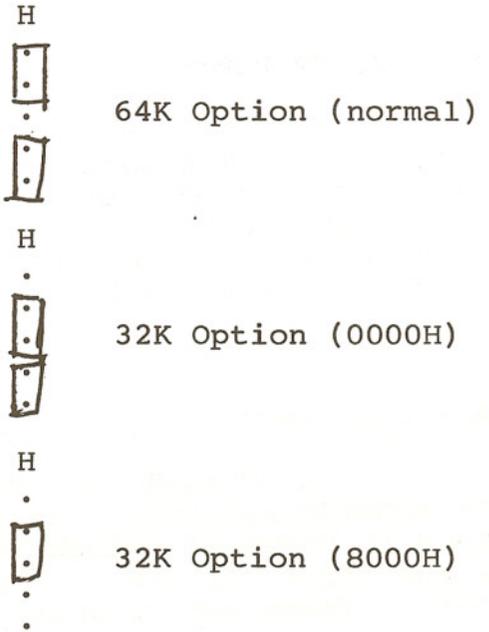
FRONT PANEL OPTION:

To enable the IMSAI front panel to write into the OMNIRAM from the front panel switches, short the left two pins in jumper area A. To disable this function short the right two pins in area A. The IMSAI front panel will read the contents of the OMNIRAM even if this option is disabled. It is recommended that this function be disabled if operation of the front panel is not required.

A   front panel enabled

A   front panel disabled
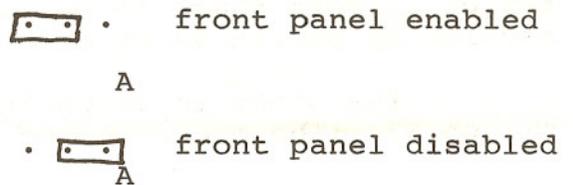
BANK SELECT OPTION:

To enable bank select-type extended addressing via an IO port short the right two pins in jumper area B. To disable ALL bank select functions, short the left two pins in jumper area B. One or the other of these options MUST be selected. If the bank select option is disabled, none of the bank-select switch settings have any effect on the operation of the OMNIRAM. If the bank select option is not desired, integrated circuits U3,U4,U5,U6,U7, and U18 may be removed. This will reduce the power consumed by the OMNIRAM.

B   bank select enabled

B   bank select disabled
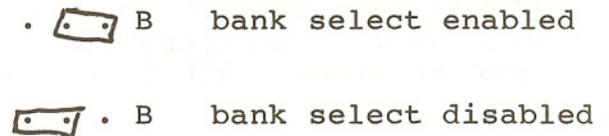
BANK SELECT PORT:

The IO port address of the bank select function is chosen by dip switch S1. The position of switch section S1-1 determines the least signifiant address of the the bank select port while S1-8 determines the most significant address. If a switch is ON (closed), logical value 0 is selected. For example, a common bank select IO port is 40H. To select this port, turn ON sections 1,2,3,4,5,6, and 8 of switch S1 and turn OFF section 7.

BANK OCCUPANCY:

The OMNIRAM is divided into two sections, a HIGH ADDRESS section and a LOW ADDRESS section. The high address section is 32K in length extending from 8000H to FFFFH if switch section S2-8 is ON. The section is 16K in length of switch S2-8 is OFF. The low address section occupies the portion of the address space not occupied by the high address sectin.

The banks in which the low address section is located are selected by switch S4. Bank-0 is selected by turning ON switch section S4-1. Bank-7 is selected by turning ON switch section S4-8. A section of the OMNIRAM may reside in more than one bank. This is accomplished by turning ON more than one section of switch S4 at one time.

The banks in which the high address section is located are selected by switch S3. The operation of this switch is similar to that of switch S4.

BANK ACTIVATION:

The two sections of the OMNIRAM can be reset to ACTIVE or DISABLED on power-on or reset. The following table illustrates the options:

	S2-1	S2-2	S2-3	S2-4
Both sections DISABLED on reset:	ON	ON	OFF	OFF
Low section ENABLED, high section DISABLED:	OFF	ON	ON	OFF
High section ENABLED, low section DISABLED:	ON	OFF	OFF	ON
Both sections ENABLED on reset:	OFF	OFF	ON	ON

Only those combinations of the switch settings shown in the above table should be used. Many 8-bit systems execute an automatic jump to a PROM at a high address such as 0C000H on reset or power-on. The disk boot routine will automatically activate the high bank on execution. For such systems, the LOW SECTION ENABLED, HIGH SECTION DISABLED option should be selected. The high bank is usually set to reside in bank-0.

DMA BANK SELECT OVERRIDE:

If DMA requests are to override the bank select feature, turn switch
5 ON. If this switch section is OFF, the board will not distinguish
between DMA transfers and HOST CPU transfers and the settings of the switches
discussed below do not affect the operation of the OMNIRAM. The transfers will
proceed according to the current bank selection status. If S2-5 is ON the two
sections of the OMNIRAM can be set to be active or inactive during DMA trans-
fers regardless of the current bank selection status. If S2-6 is ON, the
high section of the board is enabled during DMA transfers, if S2-6 is OFF, the
high section is disabled during DMA transfers. If S2-7 is ON, the low section
of the board is enabled during DMA transfers, if S2-7 is OFF, the low section
is disabled during DMA transfers.

THEORY OF OPERATION:

Because the OMNIRAM is a static memory which does not require refresh
cycles to preserve the contents of the memory, its operation is simple and
straightforward. A board select signal is generated by the 8-bit comparator
U21 which accepts inputs from sOUT, PHANTOM*, sINP, sINTA, the extended
addressing circuitry, and from the bank select circuitry. Jumpers are
provided to disable several of these inputs if required. If the 16-bit
transfer option jumpers have been installed, the board will respond to a 16-
bit transfer request by pulling S-100 buss line 60 (SIXTN*) low to indicate to
the host processer that the board is capable of making a 16-bit transfer. Note
that if the board receives a 16-bit transfer request on an odd address
boundary, it will not acknowledge the request on line 60 (SIXTN*). The INTEL
86 will not make such a request.

The OMNIRAM has two internal data busses. All of the memory chips
which are addressed when A0 is true are connected to one bus while those chips
which are addressed when A0 is false are connected to another bus.

A bipolar prom U22 receives as inputs board select, 16-bit transfer
request, A0, A15, and sMEMR. This prom arranges the internal data busses of
the OMNIRAM as required by the type of transfer. The contents of this prom
are shown on page 7. If the request is for a 16-bit transfer the cross link
between on the internal data busses U8 is disabled and the two bi-directional
buffers to the S-100 data bus are enabled. The chip-select/output enable pins
of the appropriate memory chips are activated by the four three-line-to-eight-
line decoders U1, U2, U9, and U10. If 8-bit transfers are requested, the
internal bus cross connect U8 is activated as required. Bus contention glit-
ches are avoided by enabling the S-100 bus buffers U19 and U20 only after the
internal bus connections have been established. This is possible because
sMEMR which determines whether or not the cycle is to be a READ or a WRITE is
established before pDBIN/MWRT is asserted.

Output to the bank select IO port is recognized by address comparitor
U3 in combination with sOUT and pWR*. This signal generates a clock input to
two sections of the latch U5. The state of data input to the two sections of
U5 is determined by whether or not a TRUE logic level exists on any line of
the S-100 data bus which is connected to the input of the two 8-input positive
nand gates U6 and U7 via a closed bank select switch. If this is so, the
tch assumes an active or selected state. Switch options are provided to set

the two bank select latches to the active or inactive state when POC* or RESET* are active. A bipolar prom U4 takes inputs from the two bank select latches, A15, A14, PHLDA, and three sections of switch S3. These input are used to provide a bank select qualifier to the board select comparitor U2

Use caution when removing the memory chips from their sockets. CMOS parts are susceptible to damage from static electricity.

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        MEMORY CHIP LOCATIONS ON THE OMNIRAM BOARD
              (FACE COMPONENT SIDE OF BOARD)


        3 2 1 A 8 B C D E F 1 D B C
        E E E E E E E E E E O O O O
        ---------------------------
        5 4 0 9 0 2 3 4 6 7 5 A 9 8
        E E E E O O O O O O O O O O
        ---------------------------
        6 7                     F E
        E E                     O O
```

    EVEN (E) MEANS A0 = 0 ON BYTE TRANSFERS
    ODD (O) MEANS A0 = 1 ON BYTE TRANSFERS

U22 ROM FOR THE OMNIRAM 64K MEMORY BOARD

```
-ADDRESS- + -----DATA------ + --------FUNCTION/COMMENTS----------------+
E D C B A ¶ 8 7 6 5 4 3 2 1 ¶      (BUS MASTER'S POINT OF VIEW)
---------+---------------+-----------------------------------------+
B A 1 A S ¶ D E C D O E D O ¶
S 0 6 1 M ¶ O V R I D V I D ¶
*   O 5 E ¶ E N O R D N E D ¶
    K   M ¶ N H S   L L N H ¶
    R   ¶ * I S   O O * I ¶
        ¶   * *       * ¶
---------+---------------+-----------------------------------------+
0 0 0 0 0 ¶ 0 1 1 1 0 1 1 1 ¶ BYTE-WRITE-EVEN-LOW-
0 0 0 0 1 ¶ 1 1 0 0 0 1 0 1 ¶ BYTE-READ--EVEN-LOW-
0 0 0 1 0 ¶ 0 0 1 1 0 0 1 1 ¶ BYTE-WRITE-EVEN-HIGH
0 0 0 1 1 ¶ 1 0 0 0 0 0 0 1 ¶ BYTE-READ--EVEN-HIGH
0 0 1 0 0 ¶ 0 1 1 1 1 1 0 1 ¶ WORD-WRITE-EVEN-LOW-
0 0 1 0 1 ¶ 0 1 1 0 1 1 0 1 ¶ WORD-READ--EVEN-LOW-
0 0 1 1 0 ¶ 0 0 1 1 0 0 0 0 ¶ WORD-WRITE-EVEN-HIGH
0 0 1 1 1 ¶ 0 0 1 0 0 0 0 0 ¶ WORD-READ--EVEN-HIGH
0 1 0 0 0 ¶ 0 1 0 1 1 0 1 1 ¶ BYTE-WRITE-ODD---LOW-
0 1 0 0 1 ¶ 1 1 1 0 1 0 0 1 ¶ BYTE-READ--ODD---LOW-
0 1 0 1 0 ¶ 0 1 0 1 0 0 1 0 ¶ BYTE-WRITE-ODD---HIGH
0 1 0 1 1 ¶ 1 1 1 0 0 0 0 0 ¶ BYTE-READ--ODD---HIGH
0 1 1 0 0 ¶ 1 1 1 1 0 0 1 1 ¶ WORD-WRITE-ODD---LOW- (NO RESPONSE)
0 1 1 0 1 ¶ 1 1 1 1 0 0 1 1 ¶ WORD-READ--ODD---LOW- (NO RESPONSE)
0 1 1 1 0 ¶ 1 1 1 1 0 0 1 1 ¶ WORD-WRITE-ODD---HIGH (NO RESPONSE)
0 1 1 1 1 ¶ 1 1 1 1 0 0 1 1 ¶ WORD-READ--ODD---HIGH (NO RESPONSE)
---------+---------------+-----------------------------------------+
1 0 0 0 0 ¶ 1 1 1 1 0 0 1 1 ¶ NO RESPONSE
1 0 0 0 1 ¶ 1 1 1 1 0 0 1 1 ¶ NO RESPONSE
1 0 0 1 0 ¶ 1 1 1 1 0 0 1 1 ¶ NO RESPONSE
1 0 0 1 1 ¶ 1 1 1 1 0 0 1 1 ¶ NO RESPONSE
1 0 1 0 0 ¶ 1 1 1 1 0 0 1 1 ¶ NO RESPONSE
1 0 1 0 1 ¶ 1 1 1 1 0 0 1 1 ¶ NO RESPONSE
1 0 1 1 0 ¶ 1 1 1 1 0 0 1 1 ¶ NO RESPONSE
1 0 1 1 1 ¶ 1 1 1 1 0 0 1 1 ¶ NO RESPONSE
1 1 0 0 0 ¶ 1 1 1 1 0 0 1 1 ¶ NO RESPONSE
1 1 0 0 1 ¶ 1 1 1 1 0 0 1 1 ¶ NO RESPONSE
1 1 0 1 0 ¶ 1 1 1 1 0 0 1 1 ¶ NO RESPONSE
1 1 0 1 1 ¶ 1 1 1 1 0 0 1 1 ¶ NO RESPONSE
1 1 1 0 0 ¶ 1 1 1 1 0 0 1 1 ¶ NO RESPONSE
1 1 1 0 1 ¶ 1 1 1 1 0 0 1 1 ¶ NO RESPONSE
1 1 1 1 0 ¶ 1 1 1 1 0 0 1 1 ¶ NO RESPONSE
1 1 1 1 1 ¶ 1 1 1 1 0 0 1 1 ¶ NO RESPONSE
---------+---------------+-----------------------------------------+
```

For use with CROMEMCO CDOS and CROMIX operating systems the jumper area connections are the same. These are as follows:

A □ .   B . ▱   C . ▱   D . .   E ▱   F ▱   G ▯   H . ▯

Switch settings for the CDOS system are as follows (X=either):

	S1	S2	S3	S4	S5
1	ON	OFF	ON	ON	X
2	ON	ON	ON	ON	X
3	ON	ON	ON	ON	X
4	ON	OFF	ON	ON	X
5	ON	OFF	ON	ON	X
6	ON	ON	ON	ON	X
7	OFF	ON	ON	ON	X
8	ON	ON	ON	ON	X

Switch settings for the system bank in a one user CROMIX system are as follows (X=either):

	S1	S2	S3	S4	S5
1	ON	OFF	ON	ON	X
2	ON	ON	OFF	OFF	X
3	ON	ON	ON	ON	X
4	ON	OFF	ON	ON	X
5	ON	OFF	ON	ON	X
6	ON	ON	ON	ON	X
7	OFF	ON	ON	ON	X
8	ON	ON	ON	ON	X

If the omniram is to be used with the Seattle Computer Products 16-bit 8086 system the OMNIRAM jumper areas should be connected as follows:

A . ⬚   B ⬚ .   C . ⬚   D ⬚   E . ⬚   F ⬚   G ⬚   H . ⬚
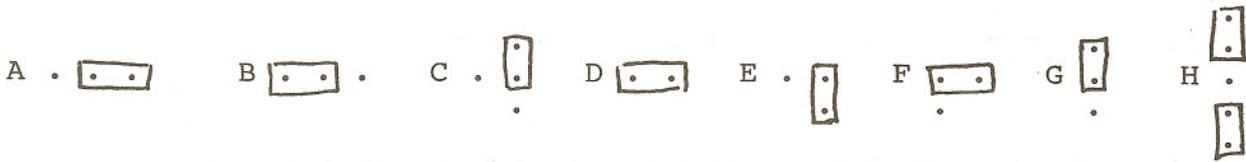
The switch settings are given below. The address of the board in this illustration begins at 00000 (X=either position).

	S1	S2	S3	S4	S5
1	ON	X	X	X	X
2	ON	X	X	X	X
3	ON	X	X	X	X
4	ON	X	X	X	X
5	ON	X	X	X	X
6	ON	X	X	X	X
7	ON	X	X	X	X
8	ON	X	X	X	X

If the OMNIRAM is to be used with the IMSAI MPU-B (8085) system without front panel the jumper settings are as follows:

A . ⬭   B ⬭ .   C ⬭   D . .   E ⬭   F ⬭   G ▯   H ▯

If the OMNIRAM is to be used with the IMSAI MPUA-A (8080) system with front panel the jumper settings are as follows:

A ⬭ .   B ⬭ .   C ⬭   D . .   E ⬭   F ⬭   G ▯   H . ▯

ALL switch settings are inoperative when using IMSAI protocal (A-16) phantom.

+5

U1
74
LS138
A12 1
A13 2
A14 3
A15 4
B3

Ø
EVEN

D0
D7

+5

U2
74
LS138
A12 1
A13 2
A14 3
A15 6
B3

8
EVEN

D0
D7

EVEN

+5

U9
74
LS138
A12 1
A13 2
A14 3
A15 4
B3

Ø
ODD

D0
D7

+5

U10
74
LS138
A12 1
A13 2
A14 3
A15 6
B3

8
ODD

D0
D7

ODD

+5

+5

S4

+5
Vcc
M58725P

A1 B   A0
A2 7   A1
A3 6   A2
A4 5   A3
A5 4   A4
A6 3   A5
A7 2   A6
A8 1   A7
A9 23 A8
A10 22 A9
A11 19 A10
        21 W
        20 OE
        GND
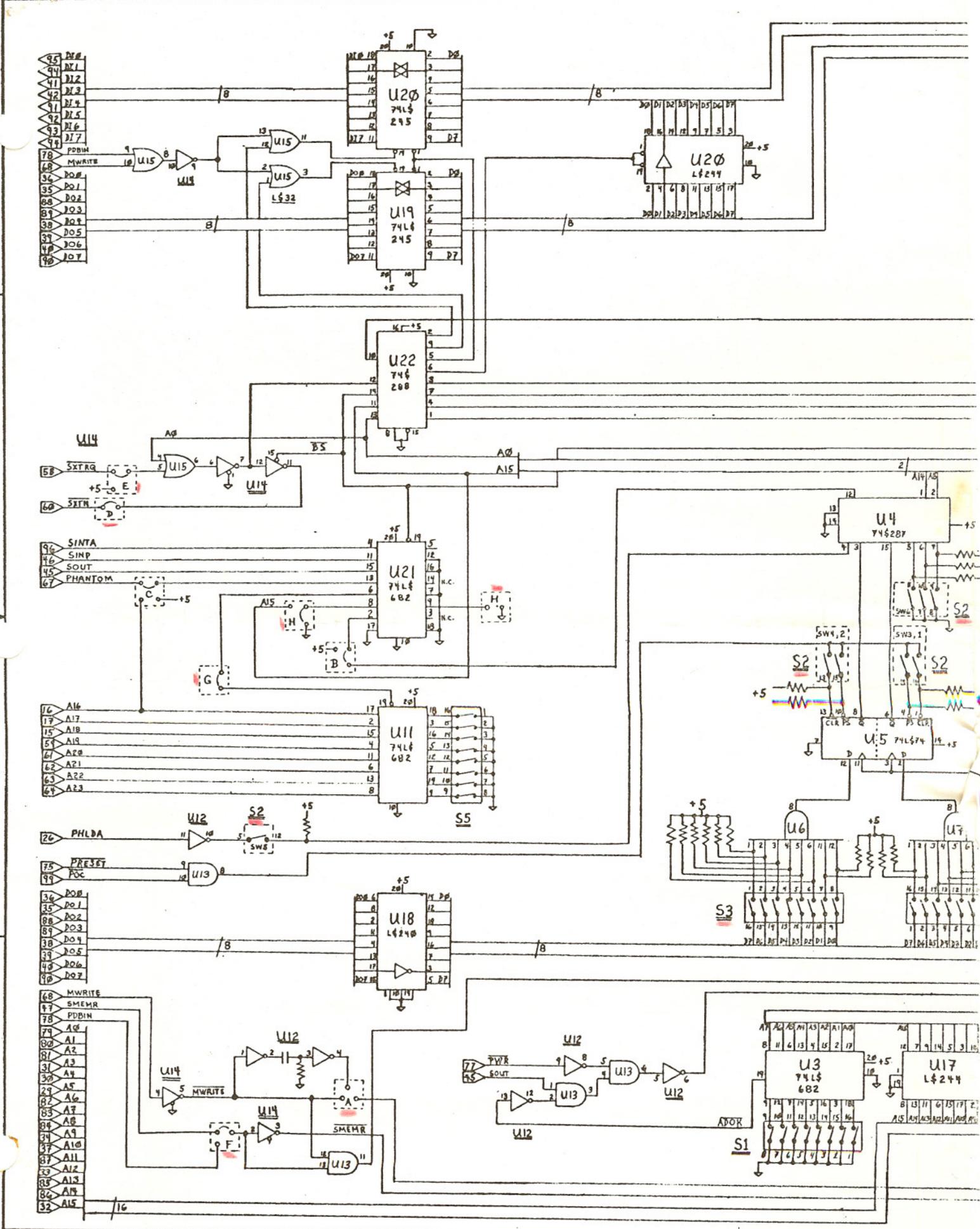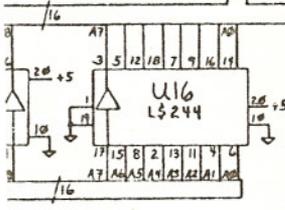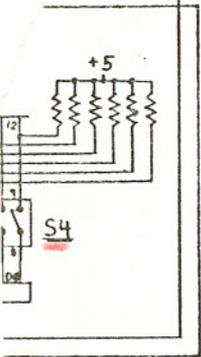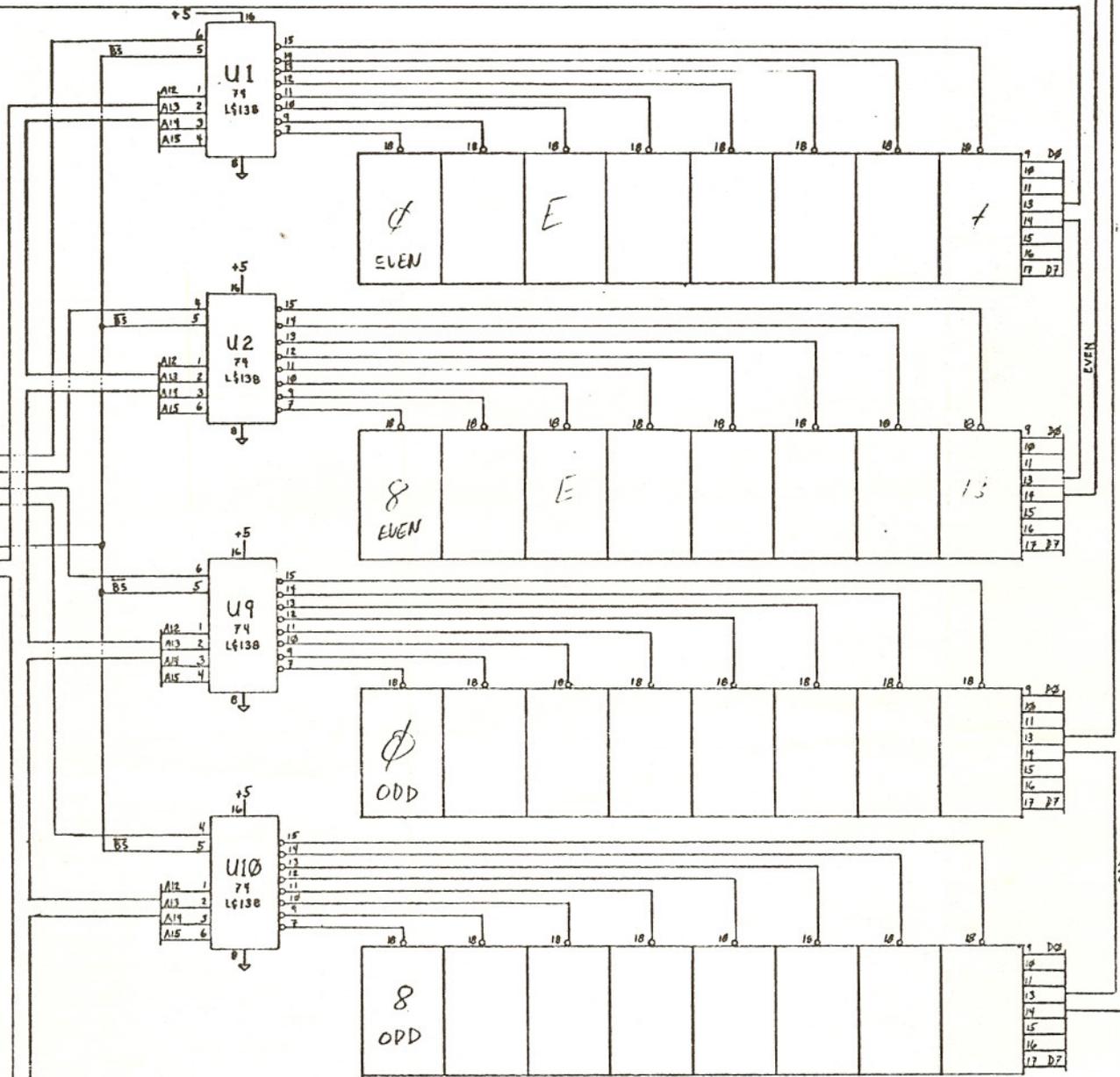
Connections Common
to all 58725's.

+5
U16
LS244

FULCRUM (EUROPE)
VALLEY HOUSE
PURLEIGH
ESSEX, ENGLAND CM3 6QH
TELEPHONE: (0621) 828763

TITLE

REV 1

CODE IDENT No   DRAWING No   REV.
27014   D
SCALE   SHEET